RAGHAV RASTOGI

raghavrastogi08@yahoo.co.in

SUMMARY:

Design and Verification Engineer with a strong knowledge of SystemVerilog, Verilog and UVM. Professional experience includes designing of Verification IP's and Verification of IP/DUT. Has completed professional degree in Electronics and Communication Engineering from Manav Rachna University, Faridabad with 9.14 CGPA.

SKILLS & INTERESTS:

Language	**:** SystemVerilog (SV), Verilog, BASH, Python, MATLAB, C.
Methodology	**:** Universal Verification Methodology (UVM).
Protocol	**:** TileLink, AMBA AXI, AHB, AXI4-Stream, MIPI DSI2, USB 3.0/3.1/3.2.
Software	**:** Cadence Xcelium, Mentor Questa, Synopsys VCS, Xilinx ISE.
ISA	**:** RISC-V.
Operating Systems	**:** Windows 10, LINUX (Ubuntu, CentOS).
Areas of Interest	**:** RTL Design, SoC, RISC-V, Automation.

WORK EXPERIENCE:

1. Company : Truechip Solutions Pvt. Ltd.
   Position : Design Engineer.
   Duration : Ongoing (May 2019 – Present).

- AMBA Team (November 2019 - Present)
  - AXI VIP (AXI 5/4/4-Lite/3)
    - Implementation of AXI5 Atomic (AWATOP) and Trace signals inside Master, Monitor, Scoreboard and Slave.
    - Addition of error injection testcases for atomic transactions and enhancing the test and sequence library of the VIP.
    - Responsible for complete customer support and bug fixes for AXI VIP.
    - Managing all the components of the AXI VIP.
    - Integration of Netspeed NoC with AXI VIP.
    - Integration of NVMe VIP with AXI VIP.
    - Integration of xHCI VIP with AXI VIP.
    - VIP enhancements as per the customer's requirements.
  - Cache Verification
    - Solely Handled the Verification of RISC-V Instruction Cache.
    - Made the verification environment from scratch.
    - Responsible for creating and coding the Master BFM, Slave BFM, Cache BFM, Cache Monitor and Cache Scoreboard.
    - Developed full test plan and verification architecture.
    - Achieved 100% code coverage and functional coverage.
  - TileLink
    - Implementation of TileLink Slave BFM.
    - Implementation of Crossbar Monitor and Crossbar Scoreboard.
    - Defined basic Architecture of the Crossbar BFM.
    - Defined TL-C Monitor checks
    - Added TL-C Testcases.

- MIPI DSI2
  - Implementation of DSI2 Receiver Layers from LM, LLP and Dummy Protocol.
  - Coding Testcases.
  - Regression cleaning and debugging.
- AXI4 STREAM VIP
  - Implementing AXI4 Stream Scoreboard.
  - Implementing Assertion Module.
  - Enhancing Coverage and achieving 100% functional coverage.
  - Adding Testcases and Sequences.
- AHB VIP
  - Enhancing the RAL model of AHB VIP.
  - Adding RAL testcases.

- USB Team (May 2019 – November 2019)
  - Debugged the USB 3.0, 3.1 Link and Phy Layers of the VIP.
  - Enhancing the VIP as per client specification.
  - Supporting client and helping them in verification of their DUT.
  - Implemented Retimer Link and Phy layer functional coverage.

ACADEMIC DETAILS:

QUALIFICATION	SCHOOL/ COLLEGE	BOARD/ UNIVERSITY	CGPA/ PERCENTAGE	YEAR OF PASSING
B. Tech (ECE)	Manav Rachna University, Faridabad	Manav Rachna University, Faridabad	9.14	2019
AISSCE	DAV Public School, Gurgaon	CBSE	70.8%	2015
AISSE	DAV Public School, Gurgaon	CBSE	74.1%	2013

PROJECTS:

1. **RISC-V based microprocessor design and verification.**
   Duration : February 2018 – December 2018.
   Technology : RISC-V RV32I and RV32M ISA, Verilog.
   A 32-bit RISC-V ISA based Microprocessor with selected instructions from RV32I and RV32M is implemented. It is a 5-stage pipelined microprocessor with external memory. The design of the microprocessor is a combination of behavioural and structural implementation, coded in Verilog. The verification of the microprocessor is done using Verilog testbenches.

CERTIFICATIONS:

1. Hardware Modelling using Verilog from IIT Kharagpur (NPTEL) in October 2018.
2. Innovations, Business Models and Entrepreneurship from IIT Roorkee (NPTEL) in October 2018.
3. Proficiency in English from Aspiring Minds in September 2018.
4. Sustainable Strategies from Purdue University in July 2016.

ACHIEVEMENTS:

1. Academic Proficiency Medal for being the Batch topper from Manav Rachna University.
2. Scholarship from Manav Rachna University.
3. Zonal Winner of BrainTech – 2017 on Networking and Cyber Security Championship organized by Azure Skynet.
4. 1st Runner up in Zenith – 2016, Hosted by Manav Rachna Educational Institution's CDC department.

HOBBIES:

- Multiplayer computer gaming (Favourite Titles: CSGO, Battlefield, Call of Duty and Tom Clancy's Universe).
- Listening to Music (Favourite Genre: Dubstep, Metal, Alternate, Pop).
- Badminton.